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2612	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/159,569	Applicant(s) SUZUKI ET AL.	
	Examiner Jason T. Whipkey	Art Unit 2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 9-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 May 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed February 11, 2004, have been fully considered but they are not persuasive.

Claims 1-6 and 9-17 are now rejected under 35 U.S.C. § 112, first paragraph, for failing to comply with the written description requirement. Consequently, the claims will be treated as if they are written to correspond to the specification. See item 3 below.

Regarding Applicant's assertion that Yamazaki teaches away from connecting one of the gate electrodes to a vertical signal line and the other gate electrode to a horizontal signal line (p. 7, para. 5), the examiner disagrees. Yamazaki does not state that the electrodes may not be connected separately to a vertical signal line and a horizontal signal line. Yamazaki is simply cited as an example of a double-gated transistor for use in the pixels of an image sensor.

In response to Applicant's argument that Yamazaki has a specific reason for using a transistor with overlapping electrodes and there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). As stated in the previous Office action, an advantage to constructing an image sensor

using double-gate transistors with overlapping electrodes is that the size of the image sensor may be reduced.

Claim Rejections - 35 U.S.C. § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. § 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-6 and 9-17 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Independent claims 1, 14, and 16 have been amended. Claim 1, for example, now recites a solid-state image pickup device, "wherein the gate electrode of one of the selection switch and the read-out switch is connected to one of the vertical signal lines". As shown in Figure 2, neither the gate electrode of the selection switch nor the gate electrode of the read-out switch is connected to vertical signal line 15. The gate electrode of the selection switch is connected to the vertical *selection* line, however. For examination purposes, the claims will be treated as if they read, "wherein the gate electrode of one of the selection switch and the read-out switch is connected to one of a plurality of vertical selection lines".

These claims also now recite a solid-state image pickup device, "wherein ... the gate electrode of the other of the selection switch and the read-out switch is connected to one of a plurality of horizontal signal lines". However, a single horizontal signal line 18 (as defined in the specification) exists in Figure 2, rather than a plurality of lines. Read-out pulse line 17 could qualify as a horizontal *selection* line, and naming it as such would maintain consistency throughout the claims. For examination purposes, the claims will be treated as if they read, "wherein ... the gate electrode of the other of the selection switch and the read-out switch is connected to one of a plurality of horizontal selection lines".

Claim Rejections - 35 U.S.C. § 103

4. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a

later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. §§ 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

6. Claims 1, 3-6, and 11-13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sauer (U.S. Patent No. 5,973,311) in view of Yamazaki (U.S. Patent No. 5,818,070).

Regarding claim 1, Sauer shows in Figure 4 a two-dimensional matrix of pixels. Each pixel, as shown in Figure 2, has a photodetector P11, such as a photodiode, to integrate photo-generated charge (column 5, lines 13-15). The pixel also includes a selection switch TR11 and a read-out switch TC11. Both switches read out the charge stored in photodetector 11 to a signal line (column 5, lines 24-27). The switches are controlled by the column select line and the row select line shown in Figure 2.

Though buffer 38 is shown to be connected to signal line 72 in Figure 4, an amplifier may also be used (column 6, lines 30-33). A separate buffer/amplifier is connected to signal line 74. The buffer/amplifier outputs an electrical signal to output signal line 30 (column 5, line 62 through column 6, line 2). Signal lines 46 and 74 have reset switches 64 and 66, respectively, for resetting the lines (column 7, lines 50-54).

Sauer is silent with regard to using a double-gated transistor in his pixels.

Yamazaki shows in figures 4B and 4C a structure that can form an image sensor (column 1, lines 33-34; column 13, lines 19-20). A dual gate (see title) CMOS circuit (column 6, line 24) includes gate electrodes 103 and 113 (column 6, line 40; column 7, lines 17-18), which are connected to first and second gate electrodes 102 and 112 (column 8, lines 35-42). First and

second gate electrodes 102 and 112 "are formed so that they substantially overlap each other" (column 2, lines 14-16).

An advantage to constructing double-gate transistors with overlapping electrodes is that the size of the image sensor may be reduced. For this reason, it would have been obvious at the time of invention to have Sauer combine the two transistors in each pixel into a single double-gate transistor with overlapping electrodes.

Regarding claims 3 and 4, Sauer teaches that the signal lines are reset before readout from the pixels begins (column 7, lines 61-64).

Regarding claim 5, Sauer shows in Figure 2 that two switches TC11 and TR11 are connected in series between photodetector P11 and the signal line.

Regarding claim 6, Sauer shows in Figure 2 that selection switch TR11 is on the side of the photodetector P11.

As for claim 11, Sauer teaches that switches 40 and 44 are provided between signal lines 72 and 74, respectively, and output line 30. Since switch 40, for example, is turned on by row select line 26 and resetting of the signal line 46 is performed when charges are not being output to it (column 7, lines 61-64), resetting of signal line 46 must occur when switch 40 is off. Therefore, switch 40 allows signal line 46 to reach a reset level during a reset time by not connecting the line to output signal line 40. Additionally, switch 49 must output the signal from buffer/amplifier 38 to output signal line 40 in order for the system to be useful.

Regarding claims 12 and 13, Sauer teaches that a correlated double sampling circuit may be included (column 13, lines 50-52).

7. Claim 2 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Sauer in view of Yamazaki and further in view of Gowda (U.S. Patent No. 5,898,168).

Claim 2 may be treated like claim 1. However, both Sauer and Yamazaki are silent with regard to using a hole accumulation diode sensor structure.

Gowda discloses a pixel circuit for an image sensor. A photodiode 26 is shown in Figure 3B. Photodiode 26 may be a pinned photodiode (column 7, lines 9-10). Official Notice is taken that a pinned photodiode is the same as a hole accumulation diode. As described in column 7, lines 18-21, the advantage of using a pinned photodiode is that it does not need to be reset after each read. For this reason, it would have been obvious for Sauer to include a pinned photodiode, such as the one described by Gowda.

8. Claims 9 and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sauer in view of Yamazaki and further in view of Munier (4,609,824).

Claim 9 may be treated like claim 1. However, both Sauer and Yamazaki are silent with regard to connecting the read-out switch between the photodetector and the signal line and connecting the selection switch to a control electrode of the read-out switch and a read-out pulse line.

Munier shows an image sensor in Figure 2 with read-out transistor $T_{1,12}$ connected between photodiode D_{12} and electrode S_2. Selection transistor $T_{2,12}$ is connected to the control electrode of transistor $T_{1,12}$ and address line Y_3.

An advantage to this transistor configuration is that random pixel access is possible. For this reason, it would have been obvious for Sauer's pixel matrix to utilize the transistor configuration taught by Munier.

Regarding claim 10, Sauer, Yamazaki, and Munier are silent with regard to using a depression MOS transistor as the selection switch.

Official Notice is taken that depression-type MOSFETs require a lower voltage across the source and drain. Therefore, the advantage to using a depression-type MOSFET is that it has reduced power requirements. For this reason, it would have been obvious to have Munier's selection switch use a depression-type MOSFET.

9. Claims 14-17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sauer in view of Yamazaki and further in view of Koch (U.S. Patent No. 4,628,364).

Regarding claim 14, Sauer shows in Figure 4 a two-dimensional matrix of pixels. Each pixel, shown in Figure 2, has a photodetector P11, such as a photodiode, to integrate photo-generated charge (column 5, lines 13-15). The pixel also includes a selection switch TR11 and a read-out switch TC11. Both switches read out the charge stored in photodetector 11 to a signal line (column 5, lines 24-27). A correlated double sampling circuit may also be included in the system (column 13, lines 50-52).

Sauer is silent with regard to using a double-gated transistor in his pixels.

Yamazaki shows in figures 4B and 4C a structure that can form an image sensor (column 1, lines 33-34; column 13, lines 19-20). A dual gate (see title) CMOS circuit (column 6, line 24) includes gate electrodes 103 and 113 (column 6, line 40; column 7, lines 17-18), which are

connected to first and second gate electrodes 102 and 112 (column 8, lines 35-42). First and second gate electrodes 102 and 112 "are formed so that they substantially overlap each other" (column 2, lines 14-16).

An advantage to constructing double-gate transistors with overlapping electrodes is that the size of the image sensor may be reduced. For this reason, it would have been obvious at the time of invention to have Sauer combine the two transistors in each pixel into a single double-gate transistor with overlapping electrodes.

Sauer is also silent with regard to outputting a reset level followed by a signal level and calculating the difference between the two.

Koch discloses a two-dimensional image sensor (Figure 1) with a pixel configuration similar to Sauer's. Koch's sensor performs correlated double sampling. In a reset state, the output of the pixels in the first sensor column, for example, is placed on line SP1, which is connected to horizontal line AL by transistor ST1 (column 5, lines 34-45). This reset signal is processed by the CDS circuitry shown in Figure 3. Actual sensor signals, including noise, are output similarly using the same circuitry (column 5, lines 49-55). The CDS circuitry then calculates the difference between the two signals to output a "clean" image signal (column 5, lines 55-58).

An advantage to performing correlated double sampling using common circuitry for transferring both reset and signal outputs is that less circuitry is needed in the pixel area of the sensor while improving image quality. For this reason, it would have been obvious at the time of invention to have Sauer's sensor use shared circuitry to perform correlated double sampling, such as that described by Koch.

Regarding claim 15, Sauer discloses that output signal line 1 and output signal line 2, which are adjacent, may be enabled simultaneously (column 9, lines 11-12). Two pixels on the same output signal line may also be enabled simultaneously (column 9, lines 1-4). This process is shown in Figure 7.

Claim 16 may be treated like claim 14. However, Sauer is silent with regard to using an optical system.

Official Notice is taken that optical systems are commonly associated with image sensors. The advantage to using an optical system with an imager is that images from a distance may be captured with great detail. For this reason, it would have been obvious to have Sauer's pixel matrix include an optical system.

Regarding claim 17, Sauer discloses that output signal line 1 and output signal line 2, which are adjacent, may be enabled simultaneously (column 9, lines 11-12). Two pixels on the same output signal line may also be enabled simultaneously (column 9, lines 1-4). This process is shown in Figure 7.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 C.F.R. § 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason T. Whipkey, whose telephone number is (703) 305-1819. The examiner can normally be reached Monday through Friday from 8:30 A.M. to 6:00 P.M. eastern daylight time, alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R. Garber, can be reached on (703) 305-4929. The fax phone number for the organization where this application is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JTW

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May 3, 2004

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